

# Protection of Digitally Controlled Inverter Units in Rapid Prototyping Applications

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**Abstract** – Mandatory and optional protection features of a modular power electronic inverter unit are described. Special attention is paid to the potential of using the digital system processing core in the implementation of these protection features. It is shown, however, that in Rapid Prototyping (RP) systems, there is an interesting option of using a digital interface between the RP system and the inverter to implement the protection features. Experimental results verify that such an interface enables the use of the inverter unit in system development based on hardware-in-the-loop (HIL) without the need for elaborate system simulations or validation, cutting development time considerably.

## I. INTRODUCTION

Many digital universal control systems are on the market today that lend themselves very well to rapid prototyping (RP) of control systems. These systems have digital output signals that must be interfaced to the IGBT gate drivers of an inverter. Analog current and voltage measurements are fed back to the controller in order to close the control loop.

In this way, a hardware-in-the-loop (HIL) test setup is created, which complements or even replaces simulations, especially in systems containing components that are very difficult or even impossible to model.

An example of such a system is the low-voltage distribution grid in distributed generation (DG) applications. The goal of these applications is to inject energy from small renewable sources at many locations in the grid and much research is still needed to ensure overall system stability and limited harmonic emission. The presence of many unknown, nonlinear loads in a grid makes simulation of the electrical subsystem quite complicated and time-consuming [1]. Combined with the variation of the complex grid impedance, one often has to start lab experiments with a probable risk of running into instabilities in mind. Obviously, reliable power converter protection at grid level voltages is very important during the development of a new DG application.

This paper describes the design of a protection system for modular voltage source inverters (VSI) used in RP systems. In Section II, the typical architecture of an RP system is described. Due to the all digital implementation of such systems, special attention is paid to the use of the digital processing core for protection. Section III lists the desirable protection features and indicates a suitable way of implementing them. Section IV deals with the actual implementation of the protection features. For RP systems,

various reasons exist to consider a stand-alone, hardware-based architecture instead of an embedded system approach. Section V describes the experimental results obtained during operation of the inverter unit. It shows the protection system behavior under overcurrent and short-circuit conditions. References are also given to working systems, constructed with the inverter unit, clearly indicating how this the protection system has become a key component in the RP systems used at the author's University power electronic lab.

## II. DIGITAL POWER CONVERTER ARCHITECTURE

### A. General

Fig. 1 shows the general layout of an all-digital power control system. This layout is typical for both motor drive and grid-coupled applications [2][3][4]. In this architecture, an instruction based digital signal processor (DSP) is complemented by peripheral hardware. In RP and development systems, the processor is usually a generic CPU or DSP, along with reconfigurable logic (FPGA) to implement the peripherals, whereas in production systems, parts or all of the components shown in Fig. 1 may be integrated in one chip or printed circuit board.

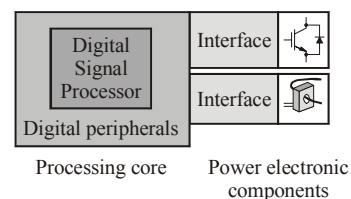


Fig. 1: All-digital power electronic control system.

The RP system described in [3][5] is entirely based on Fig. 1 and exclusively uses 3.3 V digital signals to interface reusable inverter, measurement and communications modules to a DSP/FPGA processing core. This paper actually describes the digital interface unit that is a key component of the 'Half Bridge Module (HBM)'. The HBM is the core of the modular inverter system and contains 2 IGBTs along with their galvanically isolated drivers and 2 freewheeling diodes, as shown in Fig. 2.

At the left side is a fully reconfigurable digital controller. Programming is done by describing data flow in e.g. MATLAB / Simulink. The software is subsequently generated by compilers (for either microprocessors or digital

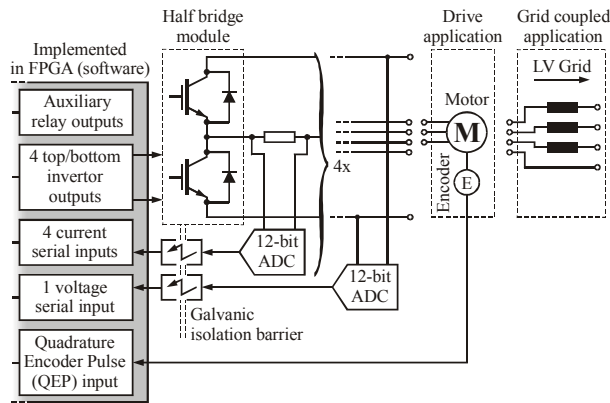


Fig. 2: Half Bridge Module (HBM) in a Rapid Prototyping (RP) system.

signal processors (DSP) or programmable logic devices such as FPGAs) and may contain errors. Such errors originate from incorrect source code (programs, logic or data flow schematics) but also from compiler bugs. In fact, the possible occurrence of these errors is one of the main reasons a protection unit was needed, especially if parts of the FPGA code are resynthesized in every software build cycle.

### B. Protection system requirements

From the introduction and the general architecture outline, it is clear that a good protection system must have the following properties.

1. It must provide a high degree of robustness against damage, both in the inverter unit and the system connected to it;
2. It must provide a high degree of robustness against improper control signals. As described above, such signals may result from a controller system crash and include stuck (high or low) and oscillating (in the MHz range) digital signals;
3. It must not introduce additional timing constraints (delays) in the signals from the digital controller. Such delays complicate the digital interface and control loop design. It will also impede a quick transition to an embedded system, in which the protection unit is removed and the protection functionality is transferred to the controller. This feature is important in industrial development;
4. It must provide personal safety, by implementing e.g. an emergency stop button.

### C. Architectural benefits to protection

In the design of a protection unit in the RP architecture, it is important to recognize that the use of fast analog-to-digital converters (ADCs) in modern RP systems has increased the number of ways that signal value checking can be implemented. These signals include the dc bus voltage, heatsink temperature, IGBT switching frequency, and output current, the latter probably being the most

important. In the design of the protection unit, three possible ways of limit checking were considered:

1. *Analog hardware* – The signal is continuously compared (after optionally being rectified) to a limiting value. The speed is in the sub-microsecond range;
2. *Digital hardware* – The signal is converted using a fast ADC. The conversion time is in the microsecond range if the ADC data stream is processed by an FPGA;
3. *Software* – The same ADC data (most likely downsampled) or data from a slower ADC is used from the digital hardware. Response times are in the sub millisecond range if processed by a fast CPU or in the millisecond range if processed by a microcontroller type of processing device.

These three methods must be kept in mind when deciding on a method to implement the features that are listed in the next section.

## III. PROTECTION FEATURE DETAILS

Considering the requirements under section II.B, the following error conditions were selected for detection in the protection unit.

### A. Excessive output current

Excessive switch current with subsequent thermal damage is probably the most important condition to check for, especially in grid-coupled VSIs (e.g. active filters) having only a very limited amount (a few mH) of inductance between the output and the grid. Three levels of protection are considered.

1. *Soft current limiting* is useful to protect the external circuits, which (usually) are more tolerant to overload (motors, inductances, transformers, etc.).
2. *Hard current limiting* is needed to protect the switches from excessive current which cannot be sustained longer than one sample period of the soft current limit checking system. The response time must be in the microsecond range.
3. *Short-circuit protection* is useful in to protect against the consequences of wiring errors. The response time must be shorter than 4 or 10  $\mu$ s, depending on the short-circuit rating of the IGBTs used. It was shown earlier [2] that a sampling digital system is capable of reacting within this time frame, albeit at a high hardware cost.

Special attention must be paid to immunity against Electromagnetic Interference (EMI), which is considerable during a short-circuit condition at full dc bus voltage.

Freewheeling diodes cannot be adequately protected against overload in the VSI circuit. It is debatable whether or not a relay or contactor should be used for this purpose, as it is likely to be too slow to prevent semiconductor damage and there is the risk of arcing when the switch is opened during a fault current.

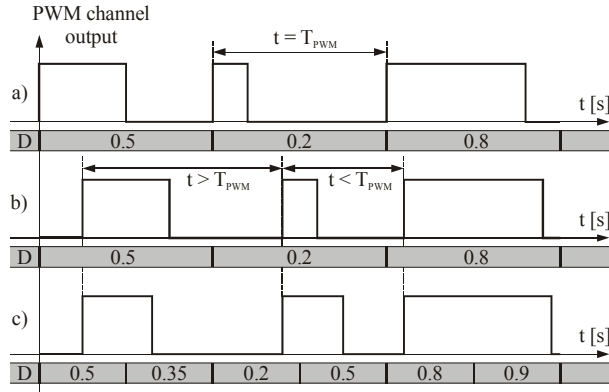


Fig. 3: Excessive Switching Frequency (ESF) detection relies on 2 measurements of  $t$ . a) Asymmetric PWM. b) Symmetric PWM. c) Doubly updated PWM.

### B. Excessive switching frequency

The power loss in an IGBT during switching is not negligible and linearly depends on the switching frequency  $f_{PWM}$ . Because the modular inverter has been used for implementation of hysteresis band type current controllers [2][6] which are implemented on the FPGA, additional verification of the maximum switching frequency was desirable. Excessive switching frequency (ESF) can be detected using a semaphore (mutually exclusive counter), which is decremented on every low-to-high transition of the HBM PWM input. A likewise transition on the reference signal  $f_{PWM,MAX}$  increments the semaphore back to 1. A semaphore count of 0 indicates an ESF condition. This type of frequency detection fails on PWM signals with varying duty cycle (Fig. 3) unless the semaphore count limit is increased to 2, as indicated in Fig. 4.

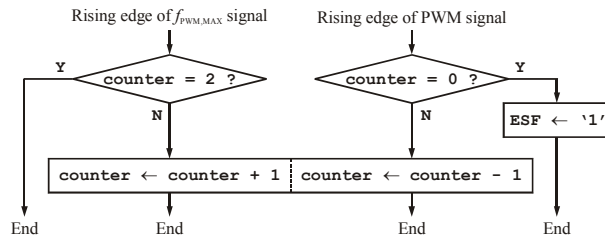


Fig. 4: ESF detection algorithm.

### C. Temperature

Only the heatsink temperature can be accurately monitored. The accurate limitation of IGBT junction temperature  $T_J$  is difficult to carry out. In fact, the two checks above (current and switching frequency) are both aimed at keeping  $T_J$  under control on a (sub-) millisecond scale. To an extent,  $T_J$  also depends on the inverter dc bus voltage. The heatsink temperature can be monitored in software.

### D. Excessive dc bus voltage

The dc bus capacitor in a VSI impedes sudden changes of the dc bus voltage. Because a margin of at least 100 V is

needed to allow for oscillations following a turn-off due to a short-circuit, protection by software is adequate.

### E. Dead time

Dead time is the time during which the top and bottom switching devices in the HBM are off. Two methods may be used to ensure that a minimum dead time is inserted.

1. Measurement of the dead time.
2. Generation of the dead time in the inverter protection unit itself.

The latter method is the easiest to implement but it is not suitable for multilevel converters. Both dead time measurement and generation require the use of digital hardware.

### F. Emergency stop

This button should never be an input of the control system under test. For personal safety, this button switches off the output contactor of the inverter system as well.

### G. Activation sequence

To ensure the proper activation, it is required that the enabling of the inverter system is event-driven (e.g. edge-triggered) and not dependent on a static signal level. This feature is also indispensable for the development of grid-coupled applications.

## IV. PROTECTION UNIT ARCHITECTURE

The set of features described above could be added to the existing signal processing core. There are three disadvantages to this approach, leading to the decision to include the protection features in the inverter module.

1. The FPGA code generation and simulation are complicated and take more time to complete.
2. If a non-trivial limit is involved, such as the derivation of the maximum current depending on maximum switching frequency, supporting software is also

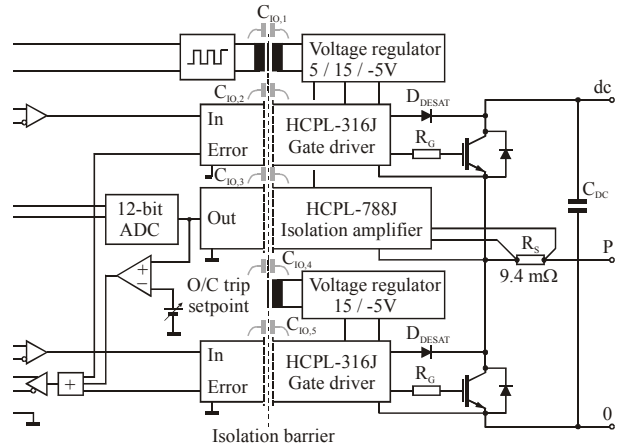


Fig. 5: Simplified HBM schematic.

needed on the system CPU.

- Software errors could potentially compromise system integrity. Even worse, in the case of software running on the CPU, errors in parts not relating to protection could prevent a protection process from running.

Part of the protection and measurements are located in the IGBT driver HBM boards, a simplified schematic of which is shown in Fig. 5. Commercial gate driver chips are used, containing a desaturation protection system monitoring the IGBT collector voltage. This system plays a major role in short-circuit handling (III.A1). A companion isolation amplifier measures the output current across a shunt and provides the current signal to the overcurrent (O/C) comparator and a 12-bit ADC. This setup minimizes the footprint of the analog section in order to reduce the noise pickup as encountered in [7] and [8].

The comparator implements the hard overcurrent function (III.A2). Although, as explained in III.A3, a single digital system could implement the soft-, hard- and short-circuit limiting functions at once, the existing HBM did not support this at the time, and it is difficult to combine with the ‘snooping’ scheme which will be explained shortly. Nevertheless, a new design should definitely consider this option. Differential signaling is used between the HBM and the control unit to avoid EMI.

The control unit consists of a Complex Programmable Logic Device (CPLD) and a small microcontroller. Fig. 7 shows the functional diagram of the control unit. The CPLD acts as a programmable signal router between the HBMs and the digital RP control system and takes care of all other functions in III.

The control unit does not perform measurements by itself. Instead, it monitors the digital ADC data channels to the FPGA, ‘stealing’ or ‘snooping’ the measurement data. If the FPGA is not initiating or performing any measurements, the inverter does not run. In this way, the protection unit runs synchronously to the RP system, minimizing complexity and delay.

The use of a microcontroller allows the reduction of the soft current limit when the allowable switching frequency is increased and vice versa. In this way, a high degree of ‘bullet-proofness’ is achieved without putting too conservative hard limits on the inverter rating.

By combining the control unit (Fig. 7) and 4 HBMs in one enclosure, a safe and compact module is obtained, as shown in Fig. 8. This particular, four channel unit is rated at 360 V, 16 A and it is based on the third generation HGTG12N60C3D IGBT component.



Fig. 7: Rear view of control and protection unit.

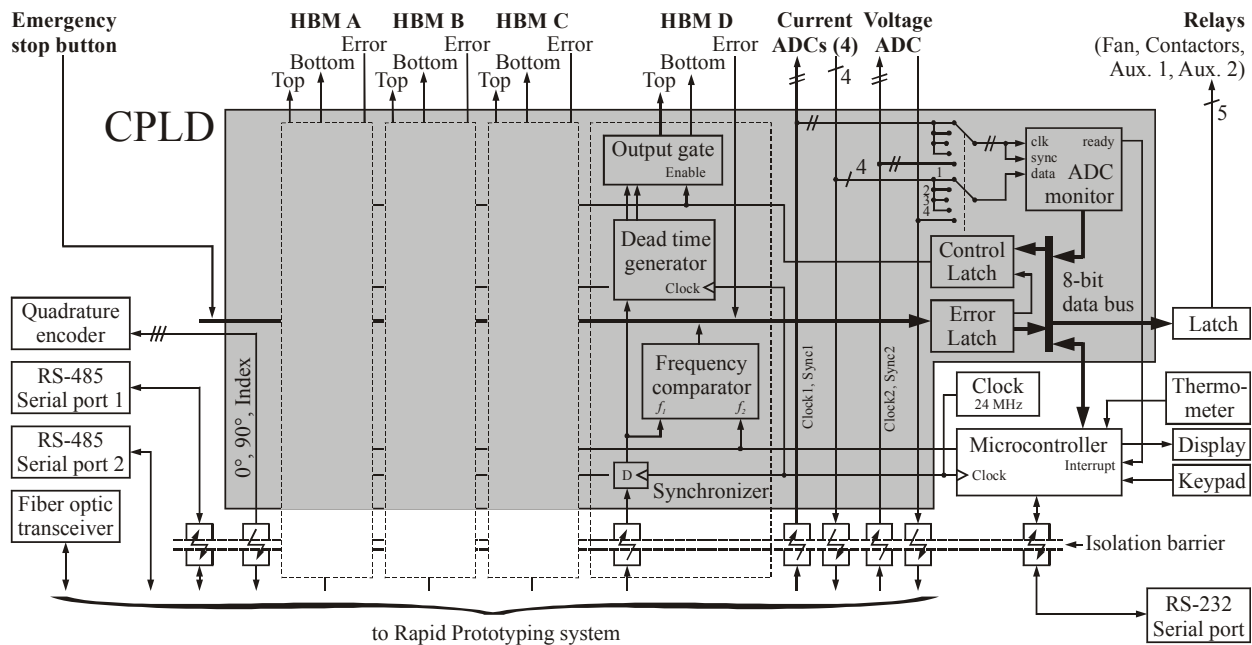


Fig. 6: Simplified control and protection unit schematic.

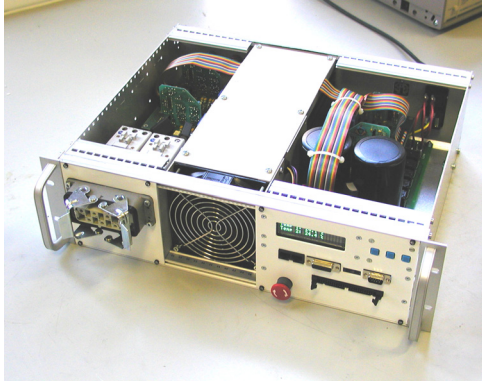


Fig. 8: Assembled modular inverter unit.

## V. EXPERIMENTAL RESULTS

### A. Current overload tests

The correct operation of the protection unit was mainly verified by overcurrent tests. All tests were conducted with a dc bus voltage of 360 V and heatsink at 25 °C. The test circuit is depicted in Fig. 9. By choosing an appropriate value of  $L$ , the rate of current rise is programmed to test a particular current limiting system. Then, the inverter is switched on (switches T1 and T4) until the overcurrent condition occurs and the protection system intervenes.

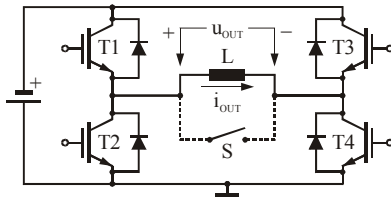


Fig. 9: Current overload measurement setup.

The *soft current limit* test is performed with  $L = 450$  mH. Fig. 10 shows the histogram of response times of 60 trials. The response is within 4.2 to 6.0 ms, the delay being due to a three tap FIR filter in the microcontroller.

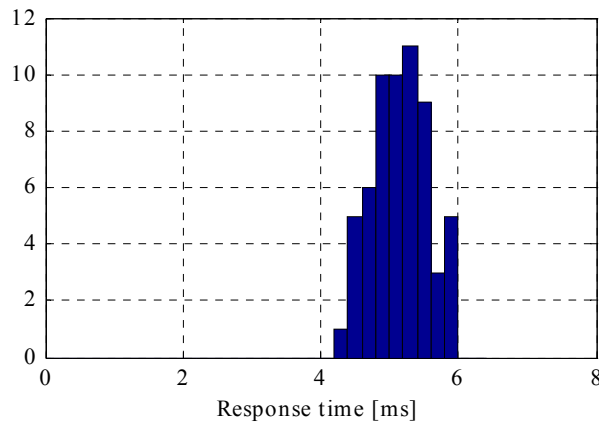


Fig. 10: Response time histogram for soft current protection.

The *hard current limit* test is performed with  $L = 150$  mH and  $L = 5$  mH. Fig. 11 and Fig. 12 show the output currents and voltages. The dashed line indicates the O/C setpoint (8.9 A). From the overshoot in Fig. 12, the delay is about 10  $\mu$ s.

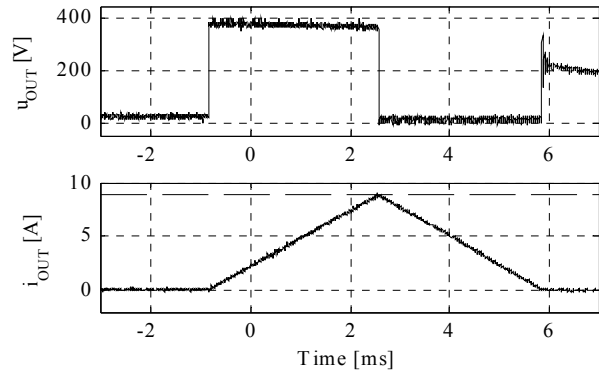


Fig. 11: Hard current limit response. ( $L = 150$  mH).

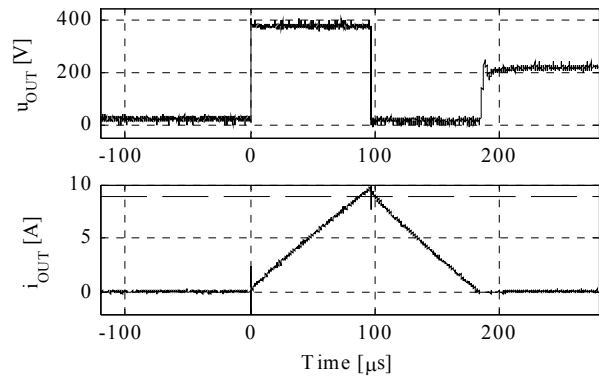


Fig. 12: Hard current limit response. ( $L = 5$  mH).

The *short-circuit* test is performed with  $L = 50$   $\mu$ H. Fig. 13 shows a response time of less than 3  $\mu$ s. The short circuit test is also repeated with a switch S instead of an inductance L. Fig. 14 shows correct operation of the protection circuit when the switch is closed *before* the inverter is turned on. Fig. 15 shows an even shorter response when the switch is closed *after* turning on the inverter output. In this case, the blanking time in the driver circuit after turn-on has already elapsed.

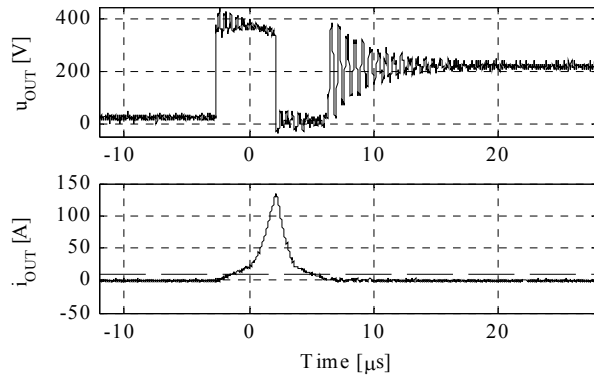


Fig. 13: Short-circuit response. ( $L = 50 \mu\text{H}$ ).

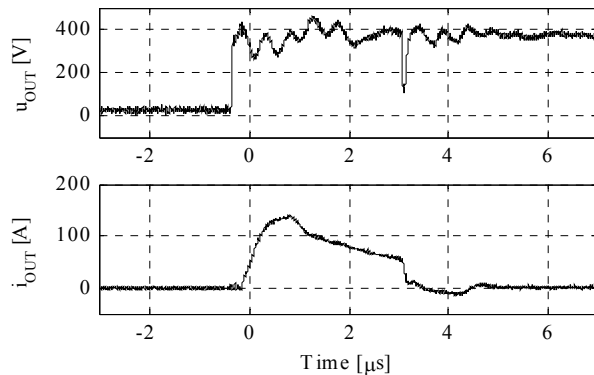


Fig. 14: Short-circuit response. Switch S is closed *before* inverter is enabled.

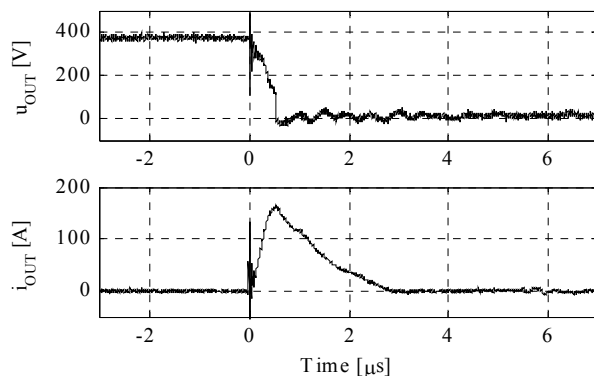


Fig. 15: Short-circuit response. Switch S is closed *after* inverter is enabled.

Note that  $i_{\text{OUT}}$  output current readings above 100 A are outside the specified range of the equipment used (Tektronix A6303). The  $u_{\text{OUT}}$  voltage measurements were performed with a Sony-Tektronix A6909 isolation amplifier.

### B. Dead time verification

Fig. 16 shows the gate signals of T1 and T2 (Fig. 9). These measurements also indicate the gate voltage levels (+13.7 / -4.7 V) and dead time (625 ns) used during the preceding current overload tests.

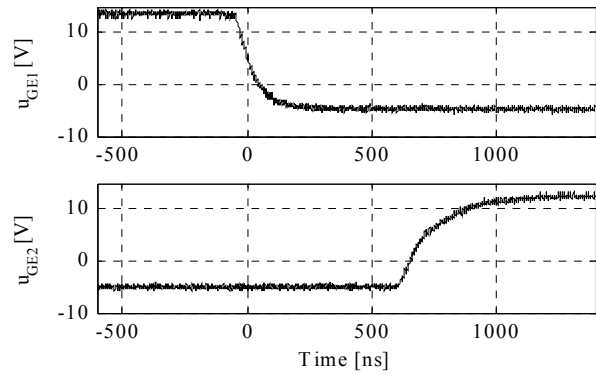


Fig. 16: Digital 625 ns dead time generation.

### C. Research references

The inverter system, including its control and protection unit, has been used in numerous, highly diverse research applications over the last two years [6][9-13]. During the development of these applications, simulations have only been carried out to validate the core components of these designs. It generally took about one day to deploy the system in real-time, during which, however, the protection unit was heavily relied upon.

### D. Student labs

Fig. 17 shows a setup implementing Field Oriented Control (FOC) of an induction machine. The motor is meant for traction purposes and is rated at 130 V, 22 A rms (5 kW) peak. This particular setup is heavily used in a student lab [13]. The short cycle from data-flow based design to working prototype ensures that students do not need to become familiar with embedded programming, stay interested, and keep their focus on control system design.

### E. Damage reports

Two cases of damage have occurred so far in the four units in use at the time of writing. In the first case, the thermally conductive pads of the 2 IGBTs accidentally overlapped under one of the IGBT packages and the HBM failed due to excessive temperature. In the second case, the freewheeling diodes were destroyed by connecting the inverter to the 230 V grid without precharging the dc bus.

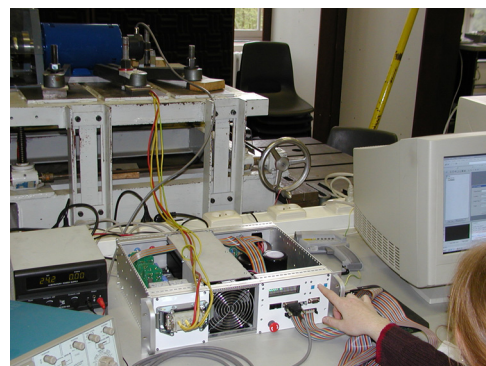


Fig. 17: Student setting soft current limit.

## VI. CONCLUSION

A simple yet effective design is proposed to adequately protect the modular inverter unit used in a rapid prototyping system for power electronics applications. An important requirement for this architecture is the all-digital implementation of the rest of the measurement and control system.

Numerous realized applications show that it is worthwhile to spend some time implementing an adequate interfacing and protection unit, because it allows skipping time-consuming simulations, which are, in many cases, difficult or even impossible to carry out. In this view, the protection unit becomes a key element in an effective and efficient power electronics development system.

## VII. ACKNOWLEDGMENTS

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