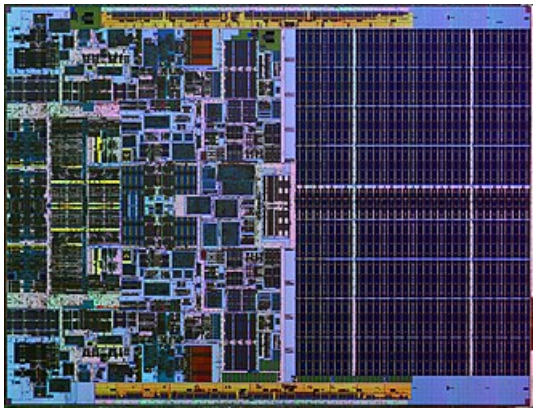
# Design of a Hardware Cost Evaluation Toolkit



Source: https://www.flickr.com/photos/187597251@N05/49996071753/

Accurate and reproducible hardware cost evaluation is essential when proposing new hardware components or security extensions for processors. However, a fair evaluation and comparison with prior art can be limited by a lack of access to specific, commercial electronic design automation (EDA) tools (Cadence, Synopsys, Siemens, ...) and their expensive licences.

Recently, the OpenROAD project[1] has made available their open-source RTL-to-ASIC EDA toolchain, which produces tapeout-ready netlists but lacks in user friendliness. Simultaneously, members of the systems security research community have proposed their own open-source evaluation toolchain[2], based on best practices from the field of cryptographic hardware[3]. The preliminary version of this toolchain is easy-to-use, but lags behind in reliability, speed and evaluation figures compared to OpenROAD tools.

In this thesis, the student will develop an easy-to-use and high-quality hardware cost evaluation toolkit, enabling meaningful evaluation and comparison of hardware designs. The goal is to distill useful features from commercial and advanced tools, and integrate them into an easy-to-use toolkit. This toolkit should support the evaluation of several metrics, including: area, clock frequency, power, and more. Furthermore, the student will analyze the performance of their toolkit through a systematic study of RISC-V-based hardware designs in the academic literature. Finally, the student can scrutinize the practices employed in published research and propose a better way forward. Through this master thesis, the student has the opportunity to contribute to the field of systems security by enabling more reproducible and fair hardware cost evaluation. The student should be familiar with the ASIC and/or FPGA design and synthesis (tool)flow.

## Practicalities


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|---|---|---|---|
| Promoter: | Ingrid Verbauwhede | | |
| | Márton Bognár | | |
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| | Quinten Norga | quinten.norga@esat.kuleuven.be | office 01.16 |
| Nature of the work: | 20% literature, 10% theoretical work, 70% implementation/experiments | | |
| Number of students: | 1 | | |


[1] https://theopenroadproject.org/

[2] J. De Meulemeester et al. 2025. Hardware Cost Evaluation in Systems Security. ACM REP '25. https://doi.org/10.1145/3736731.3746155

[3] https://github.com/KULeuven-COSIC/eval-hd

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